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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/605,408	Confirmation No. 2407
Applicant	:	Kern Rim	
Filed:	:	September 29, 2003	
TC/Art Unit:	:	2813	
Examiner	:	James M. Mitchell	
Docket No.	:	YOR920000707US2	
Customer No.	:	27127	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

DECLARATION UNDER 37 CFR §1.131

I, Kern Rim, depose and say that:

(1) I am the sole inventor of the subject matter covered by each of the claims pending in the above-identified U.S. patent application (the "Present Application").

(2) I am currently employed with International Business Machines Corp. (IBM), the assignee of the Application.

(3) Prior to February 7, 2002, I submitted Disclosure YOR8-2000-0640 (the "Disclosure"), attached hereto as Exhibit A, which describes the invention disclosed and claimed in the Present Application. The Disclosure was reviewed, dated and assigned docket number YOR920000707US1 by the Intellectual Property Law Department of IBM.

(4) U.S. Patent Application Serial No. 09/823,855 (the "Kern Application"), now U.S. Patent No. 6,603,156 (the "Kern Patent"), and the Present Application were filed covering the product and method, respectively, disclosed in the Disclosure. Though not filed as a divisional application, the Present Application contains the identical specification and drawings as the Kern Application and Kern Patent, the latter of which issued less than one year before the filing date of the Present Application.

(5) The Kern Application was filed on my behalf on March 31, 2001, and therefore prior to February 7, 2002. Therefore, the invention disclosed in the Disclosure, Kern Application, and Kern Patent and currently being claimed in the Present Application was both conceived and constructively reduced to practice before February 7, 2002, as shown by the filing date of the Kern Application and Kern Patent.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Kem Rim

YOR9-20[redacted]-0707

Disclosure YOR8-2000-0640

Created By: Ken Rim **Created On:** [redacted]M
Last Modified By: Ken Rim **Last Modified On:** [redacted]M

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Required fields are marked with the asterisk (*) and must be filled in to complete the form .

Summary

Status	Under Evaluation
Processing Location	YOR
Functional Area	700 Isaac-Systems, Technology & Science
Attorney/Patent Professional	Casey August/Watson/IBM
IDT Team	Casey August/Watson/IBM
Submitted Date	[redacted]
Owning Division [redacted]	RES
PVT Score [redacted]	48
Incentive Program	
Lab	
Technology Code	

Inventors with Lotus Notes IDs

Inventors: Ken Rim/Watson/IBM

Inventor Name > denotes primary contact	Inventor Serial	Div/Dept	Manager Serial	Manager Name
> Rim, Ken (Ken)	2A4817	22/K3QB	407736	Wong, H.-S. Philip

Inventors without Lotus Notes IDs

IDT Selection

IDT Team:	Attorney/Patent Professional:
Casey August/Watson/IBM	Casey August/Watson/IBM

Response Due to IP&L [redacted]

Main Idea

Title of disclosure (in English)

Structures and Methods to form Strained Si on Insulator (SSOI) for Strained Si CMOS and Other MOSFET Applications

Idea of disclosure

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.
Strained Si CMOS essentially refers to CMOS devices fabricated on a substrate that consists of a thin, (50~300 angstrom) strained Si layer typically grown on a relaxed SiGe layer. Publications both from IBM and other institutions in the past have shown the potential of achieving high electron and hole mobility in

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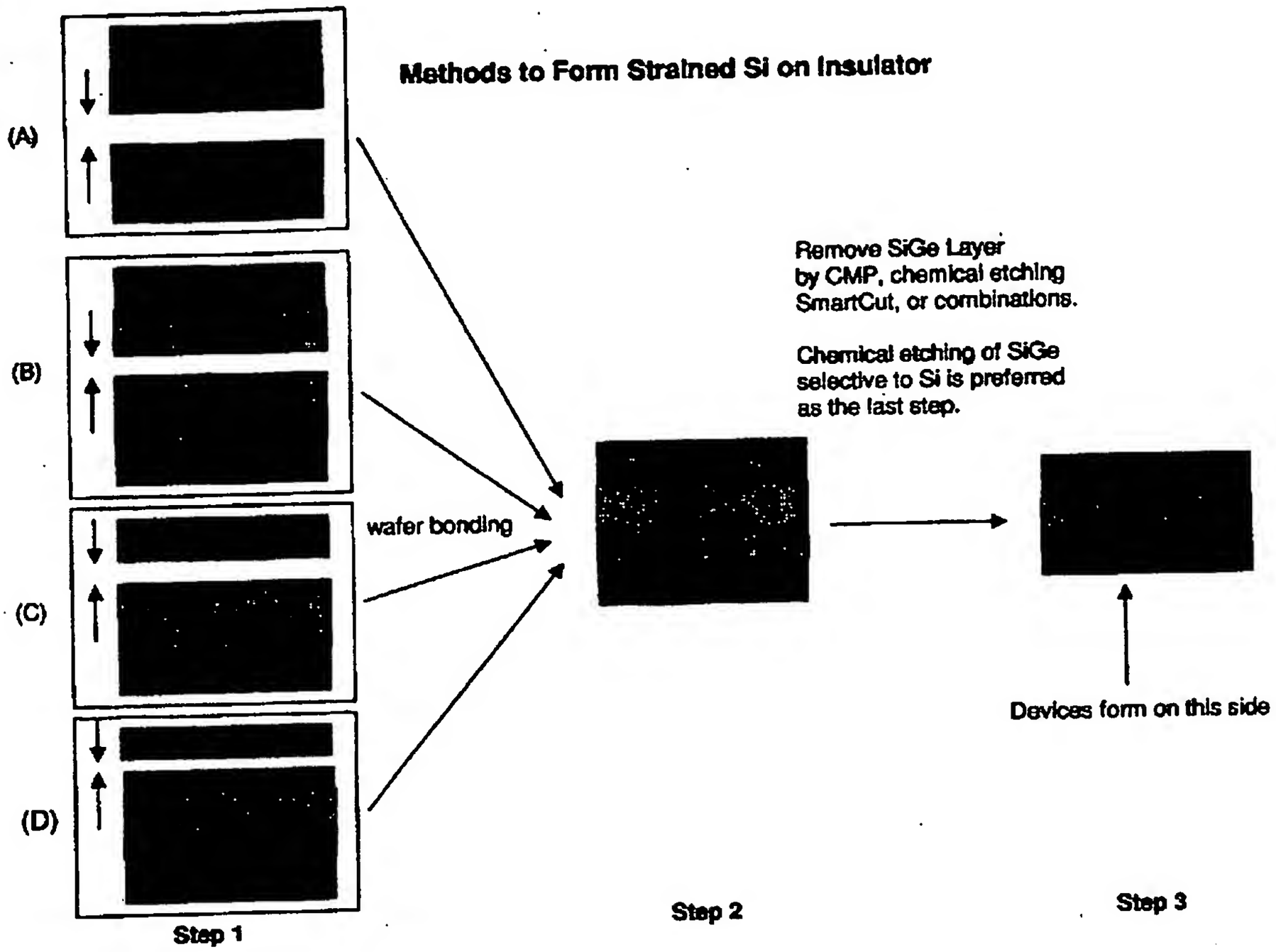

The basic structure claimed (strained Si on insulator, or SSOI) consists of a thins strained Si layer on top of a layer of insulator (SiO2, SiN, Al2O3 and other so called "high K" materials, low K materials, etc.) which in turn may be on top of a substrate material which should usually be a semiconductor (Si, poly Si, SiGe, III-V semiconductors), but can also be a conductor (metal).

Such structure can be used to form a SOI MOSFET or a double gate MOSFET (in which case the insulator layer mentioned above serves as the "back" gate insulator) using typical process steps to form such MOSFET structures.

Methods to form SSOI:
1. Strained Si layer is epitaxially grown on relaxed SiGe by known methods. The methods to form the relaxed SiGe layer (epi growth, Czhochralski growth, etc.) are not critical to this invention.

2. Optional layers of insulator (which will become the whole or part of the buried insulator layer in the final structure) or semiconductor (or conductor, which can serve as the "back gate" in a double gate MOSFET application) layers are either thermally grown or deposited on top of the Si layer.

3. The structure is bonded to a handle substrate that consists of semiconductor layers (or conductor layers) and an optional insulator layer (which will become the whole or part of the buried insulator layer in the final structure) by processes commonly known as "wafer bonding".

4. The SiGe layer is removed *completely* by processes that consist of wafer cleaving (e.g. SmartCut), chemical mechanical polishing (CMP), chemical etching. The preferred method of removing the last layers

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Strained Si on Insulator (SSOI) structure for MOSFET Applications

Basic Claimed Structure

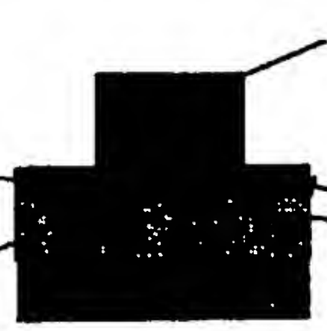
Strained Si
(under biaxial tension)
0A < thickness < 500A
$a_{in\text{-}plane} > a_{Si,equilibrium}$

Insulator
0A < thickness < 1 um (arb.)
(SiO2, SiN, Al2O3, etc.)

Semiconductor
(Si, poly silicon, SiGe, GaAs, etc.)

Applications

SSOI MOSFET (n- and p-)



Strained Si Double Gate MOSFET

Ken Rim, IBM Research

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[redacted]8-2000-0640 Structures and Meth[redacted] to form Strained Si on Insulator (SSOI) for Strained [redacted]CMOS and Other MOSFET Application - continue

such a strained Si layer. Recent publications have experimentally demonstrated strained-Si MOSFETs, and have shown that the device performance is enhanced in these structures, compared to the devices fabricated on conventional (unstrained) Si substrates. The improvements that can be achieved in such MOSFETs with strained Si channel include increased device drive current and transconductance, as well as the added ability to scale the operation voltage without sacrificing circuit speed in order to reduce the power consumption.

One of the difficulties in realizing strained-Si CMOS technology is the presence of relaxed SiGe layer under the strained-Si channel layer. The SiGe layer serves to supply the strain to the top Si layer. The interaction of the SiGe layer with various processing steps such as thermal oxidation, salicide formation, and annealing presents difficulties in maintaining material integrity during the CMOS fabrication, and can ultimately limit the device performance enhancements and device yield that can be achived. Furthermore, SiGe layer adds to the total thickness of the body region of a MOSFET (especially in SOI FET structures), and presents a disadvantage in attempts to form a very thin body SOI devices, whose merits as a MOSFET structure for very short channel lengths are well documented in literatures.

The invention disclosed in this document offers a solution to this problem by 1. a structure that**places the strained Si channel layer directly on an insulator** thereby making the insulator and the underlying material the substrate that supports the strain in the Si channel layer, 2. a preferred method to form such structure.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

Here are the figures ssoi.ppt that describe the basic structure and the methods to form it.

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of SiGe is a selective chemical etching process where SiGe is preferentially etched at higher rate than Si. If SmartCut process is to be used, the necessary hydrogen implant can be performed during various time points between step 1 and step 3.

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?
U.S. Patent 5,906,951(IBM) includes a structure that consists of strained Si on SiGe layers on insulator. The present disclosure describes a strained Si on insulator structure where the SiGe layer is completely absent.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
None

***Critical Questions (Questions 1 - 7 must be answered)**

Question 1
On what date was the invention workable? [redacted] **Please format the date as MM/DD/YYYY**
(Workable means i.e. when you know that your design will solve the problem)

Question 2 ○ Yes ● No
Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?
If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:

Are you aware of any publications, products or patents that relate to this invention? ○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:

Question 3 ○ Yes ● No
Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal?
Is a sale, use in manufacturing, product announcement, or proposal planned? ○ Yes ● No
If Yes, identify the product if known and indicate the date or planned date of sale, announcements, or proposal and to whom the sale, announcement or proposal has been or will be made:
Product:
Version/Release:
Code Name:
Date:
To Whom:
If more than one, use cut and paste and append as necessary in the field provided.

Question 4 ○ Yes ● No
Was the subject matter of your invention or a product incorporating your invention used in public e.g., outside IBM or in the presence of non-IBMers?
If yes, give a date. **Please format the date as MM/DD/YYYY**

Question 5 ○ Yes ● No
Have you ever discussed your invention with others not employed at IBM?
If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.

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